AMENDMENTS TO THE CLAIMS

Claims 1-26 (Canceled).

27. (Currently amended) An intermediate structure for an array of resistance variable memory cells ~~in an integrated circuit, at least one memory cell~~ comprising:

[a]]at least one pillar of stacked material layers on a semiconductor substrate, the stacked layers comprising a first electrode layer, a chalcogenide glass layer having metal ions diffused therein and being capable of changing resistance under the influence of an applied voltage, and a second electrode layer, ~~each layer having lateral edges, the lateral edges of each layer approximately vertically aligned with lateral edges of each other layer~~the at least one pillar not located within a via.

Claims 28-48 (Canceled).

49. (Previously presented) The array of Claim 27, wherein the metal ions comprise silver ions.

50. (Previously presented) The array of Claim 27, wherein at least one of the first and second electrodes is tungsten.